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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,407	06/25/2007	Anthony Moon	MCLRK-009US	5729
7663 7590 02/26/2009 STETINA BRUNDA GARRED & BRUCKER 75 ENTERPRISE, SUITE 250 ALISO VIETO, CA 02656			EXAMINER	
			BALDRIDGE, BENJAMIN M	
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			2831	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
	10/566,407	MOON ET AL.				
Office Action Summary	Examiner	Art Unit				
	Benjamin M. Baldridge	2831				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) ☐ Responsive to communication(s) filed on 26 Ja 2a) ☐ This action is FINAL . 2b) ☐ This 3) ☐ Since this application is in condition for allowant closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro					
Disposition of Claims						
4) ☐ Claim(s) 1 - 32 is/are pending in the application 4a) Of the above claim(s) 29, 31 - 32 is/are with 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1 - 15, 17 - 28, 30 is/are rejected. 7) ☐ Claim(s) 16 is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or Application Papers 9) ☐ The specification is objected to by the Examiner 10) ☐ The drawing(s) filed on 26 January 2006 is/are: Applicant may not request that any objection to the or	ndrawn from consideration. r election requirement. r. a) accepted or b) objected	-				
Replacement drawing sheet(s) including the correcti	on is required if the drawing(s) is obj	ected to. See 37 CFR 1.121(d).				
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 26 January 2006, 9 March 2006.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	nte				

Art Unit: 2831

.DETAILED ACTION

1. Claims 1 - 28 and 30 are presented for examination; claims 29, 31 - 32 are cancelled.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Figure 3: item 1, mentioned as part of Figure 3 on Page 9 of the specification, is not found in the drawing.

Figure 6: item 61, mentioned as part of Figure 6 on Page 12 of the specification, is not found in the drawing.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Art Unit: 2831

Specification

Claim Objections

3. Claim 8 objected to because of the following informalities:

The limitation "substantially in a parallel" is recited; the meaning of "in a parallel" is unclear. For the purposes of examination, it is assumed that the intended meaning of the phrase is "substantially in parallel".

Appropriate correction is required.

4. Claim 16 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 16 clearly further limits the subject matter of claim 15; however, the preamble of the claim reads "a capacitive sensor as claimed in claim 14. As claim 14 is drawn to a first signal that is an integrated square wave, it appears that claim 16 should depend from claim 15, and for the purposes of examination, it will be so read.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2831

6. Claims 1 – 10, 12, 17 – 18, 20 – 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Vranish (US Patent 5,373,245, December 13, 1994, hereinafter referred to as Vranish).

As to claim 1, Vranish discloses:

A capacitive sensor (Abstract, lines 1-2);

A sensor plate configured to have a first signal applied thereto (Abstract, lines 3 – 7; Figure 3a, item 12₁);

First guard plate interposed between the sensor plate and the body, which is configured to have a first guard plate signal applied thereto (Column 5, lines 25 – 30; Figure 3a, items 12, 2; note position of first guard planar electrode/plate 1);

A second guard plate interposed between the first guard plate and the body which is configured to have a second guard plate signal applied thereto (Column 5, lines 35 – 45; Figure 3a, items 2, 1, note position of second guard planar electrode/plate).

As to claims 2 – 10, Vranish discloses:

at least one control means configured to apply the first and second guard plate signals to the first and second guard plates respectively [claim 2] (Figure 2, item 28, 8; also Figure 7, where means for providing a common reference, and means for controlling thermal drift are disclosed, which are interpreted as "control means". Note that the instant claim is not considered to be in proper form for interpretation according to the provisions of 35 USC 112, 6th paragraph);

The first guard plate signal is related to the first signal applied to the sensor plate by a first amplification factor and the second guard plate signal is related to the first signal by a second amplification factor [claim 3] (Column 5, lines 30 - 37; Figure 3a, items 1, 2, 4, 4a; note signal paths from oscillator/signal source item 28 to the sensor plate and the guard plates);

The first and second amplification factors are substantially one [claim 4] (Column 5, lines 10 - 15, 30 - 32; note that the term "voltage follower" in Vranish is used to denote a unity gain buffer amplifier, as is evident from the amplifier schematics shown in Figure 3a, etc. Note also that the use of unity gain buffer amplifiers for isolation or other purposes is well known to persons of ordinary skill in the art, and would have been obvious to such persons as a routine exercise of ordinary skill);

Application/Control Number: 10/566,407

Art Unit: 2831

The first and second guard plates signals are substantially identical to the first signal applied to the sensor plate in terms of frequency, phase and amplitude. [claim 6] (Figure 3a, items 28, 4, 4a, 6₃, etc.; note that the sensor plates and guard plates are fed from a common signal source, through voltage followers (i.e. unity voltage gain amplifiers, ensuring identical frequency and phase; note also that Vranish discusses use of capacitors (Figure 6, items 20, 21₁₋₃) to eliminate phase shift between voltages measured at the output of the amplifiers):

Page 5

An insulative substrate between the first guard plate and the second guard plate, for electrically isolating the first guard plate from the second guard plate [claim 7](Column 5, line 68, Column 6, lines 1 – 8; note also that an insulator (i.e. dielectric substance) is commonly used in capacitive sensors, to separate electrodes, and its use would have been obvious to persons of ordinary skill in the capacitive sensor design art at the time of the invention, as a routine exercise of ordinary skill);

The first and second guard plates are arranged substantially in (a) parallel [claim 8] (Figure 3a, items 1, 2, clearly showing the first and second guard plates parallel to each other);

First and second amplifier units [claim 9] (Figure 3a, items 4, 4a);

The first signal applied to the sensor plate is also applied to the first amplifier unit [claim 9] (Figure 3a, item 28, 4a, 16a; note signal flow from signal source item 28 to amplifier 4a, the first amplifier unit);

The output of the first amplifier unit is fed to the first guard plate and the second amplifier unit [claim 9] (Figure 3a, items 4a, 16a, 1; note signal flow from signal source item 28),

The output of the second amplifier unit is fed to the second guard plate [claim 9] (Figure 3a, items 4, 16, 2; note signal flow).

First and second amplifier units [claim 10] (Figure 3a, items 4, 4a);

The first signal applied to the sensor plate is fed to the first and second amplifier units [claim 10] (Figure 3a, items 28, 4, 4a; note signal inputs to amplifiers 4, 4a);

The output of the first amplifier unit is fed to the first guard plate and the output of the second amplifier unit is fed to the second guard plate [claim 10] (Figure 3a, items 1, 2, 16, 16a, 4, 4a; note signal flows from amplifiers 4, 4a to first and second

guard plates, items 1 and 2);

Each amplifier has a gain of substantially one [claim 12] (Column 5, lines 10 - 15, 30 - 32; note that the term "voltage follower" in Vranish is used to denote a unity gain buffer amplifier, as is evident from the amplifier schematics shown in Figure 3a, etc. Note also that the use of unity gain buffer amplifiers for isolation or other purposes is well known to persons of ordinary skill in the art, and would have been obvious to such persons as a routine exercise of ordinary skill);

As to claims 17 - 18 and 20, Vranish discloses:

A capacitive sensor system [claim 17] (Abstract, lines 1-2);

A signal source arranged to produce a main signal [claim 17] (Figure 3a, item 28);

First and second amplifier units [claim 17] (Figure 3a, items 4, 4a);

The main signal is fed to a sensor plate connection and the first amplifier unit (Figure 3a, item 28, 12, 4; note signal paths to both sensor plates and first amplifier unit 4);

The output of the first amplifier unit is fed to a first guard plate connection and the second amplifier unit [claim 17] (Figure 3a, items 4a, 16a, 1; note signal flow from signal source item 28);

The output of the second amplifier unit is fed to a second guard plate connection [claim 17] (Figure 3a, items 4, 16, 2; note signal flow);

A capacitive sensor control system for connection to a capacitive sensor comprising a sensor plate, a first guard plate interposed between the sensor plate and the body and a second guard plate interposed between the first guard plate and the body [claim 18] (see discussion of claim 1 above, which specifies the disclosure of each element of the preamble to the instant claim);

A signal source arranged to produce a main signal [claim 18] (Figure 3, item 28);

First and second amplifier units [claim 18] (Figure 3a, items 4, 4a);

The main signal is fed to the sensor plate and to the first and second amplifier units [claim 18] (Figure 3a, item 28, 12, 4, 4a; note signal paths to both sensor plates and first and second amplifier units 4 and 4a);

The output of the first amplifier unit is fed to the first guard plate and the output of the second amplifier unit is fed to the second guard plate [claim 18] (Figure 3a,

items 4, 4a, 1, 2; note signal flows from first and second amplifiers to first and second guard plates, items 1 and 2);

Each amplifier has a gain of substantially one [claim 20] Column 5, lines 10 – 15, 30 – 32; note that the term "voltage follower" in Vranish is used to denote a unity gain buffer amplifier, as is evident from the amplifier schematics shown in Figure 3a, etc. Note also that the use of unity gain buffer amplifiers for isolation or other purposes is well known to persons of ordinary skill in the art, and would have been obvious to such persons as a routine exercise of ordinary skill).

As to claim 21, the method disclosed in the instant claims are intrinsic to the circuit and system disclosed in claim 1, as discussed above, since the method steps will be met during the normal operation of the system stated above.

As to claim 22, the method disclosed in the instant claims are intrinsic to the circuit and system disclosed in claims 1 and 3, as discussed above, since the method steps will be met during the normal operation of the system stated above.

As to claim 23, the method disclosed in the instant claims are intrinsic to the circuit and system disclosed in claims 1 and 4, as discussed above, since the method steps will be met during the normal operation of the system stated above.

As to claim 24, the method disclosed in the instant claims are intrinsic to the circuit and system disclosed in claims 1 and 6, as discussed above, since the method steps will be met during the normal operation of the system stated above.

As to claims 25 and 26, the method disclosed in the instant claims are intrinsic to the circuit and system disclosed in claims 1, 9 and 10, as discussed above, since the method steps will be met during the normal operation of the system stated above.

7. Claim 5 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Vranish.

Art Unit: 2831

As to claim 5, Vranish fails to explicitly disclose the limitation:

The second amplification factor is greater than the first amplification factor.

However, design and use of amplifiers having greater or less gain than a first amplification factor (in this case, unity) is a common practice in many electronic design arts, and would have been well known to persons of ordinary skill in the art at the time of the invention. Varying the gain of an amplifier to meet a requirement, especially an op-amp based amplifier, in which the gain is a function of the ratio of feedback and input resistors, is well within the ordinary capabilities of persons of ordinary skill in the art, and would have been seen as an exercise of routine skill in the art, requiring no special inventive step. Consequently, the limitation cannot be considered patentably distinct over the routine capabilities of persons of ordinary skill in the art.

Claim Rejections - 35 USC § 103

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 9. Claims 11, 19, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vranish in view of Hiroshima et al (US Patent 6,331,780 B1, December 18, 2001, hereinafter referred to as Hiroshima).

As to claims 11 and 19, Vranish discloses an apparatus and methods as discussed in paragraph 6 above. However, Vranish fails to disclose:

A third amplifier, wherein the first signal is fed to the first and second amplifier units via a third amplifier unit.

Hiroshima discloses:

A third amplifier, wherein the first signal is fed to the first and second amplifier units via a third amplifier unit [claims 11, 19] (Figure 4, items 25, AMP 4; Column 8, lines 29 - 31; note explicit use of buffer amplifier to isolate the signal source; note also that use of amplifiers to increase amplitude or power of signal sources is well known to persons of ordinary skill in the circuit and system design arts, and would have been obvious to such persons at the time of the invention; note also that increased signal power into the sensor and guard electrodes will allow (among other things) the use of multiple sensor electrodes and larger guard electrodes).

Given the teaching of Hiroshima, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the circuit and system of Vranish by employing well known or conventional features such as a third amplifier feeding a first and second amplifier, as disclosed by Hiroshima, in order to furnish sufficient signal power to multiple sensor elements and guard plates.

As to claims 27, the method disclosed in the instant claims are intrinsic to the circuit and system disclosed in claims 1, 9, 10 and 11, as discussed above, since the method steps will be met during the normal operation of the system stated above.

As to claims 28, the method disclosed in the instant claims are intrinsic to the circuit and system disclosed in claims 1, 4, 9, 10 and 11, as discussed above, since the method steps will be met during the normal operation of the system stated above.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vranish in view of Stanley et al. (US Patent Application Publication Pub. No. US 2001/0045733 A1, Pub. Date November 29, 2001, hereinafter referred to as Stanley).

As to claim 13, Vranish discloses an apparatus and methods as discussed in paragraph 6 above. However, Vranish fails to disclose:

Calculation means for providing proximity information based upon the capacitance between the sensor plate and electrical ground.

Stanley discloses:

Calculation means for providing proximity information based upon the capacitance between the sensor plate and electrical ground ([0058], lines 4 – 15, 18 – 20; note also that "calculation means" is construed to include items common in art, such as microprocessors, microcontrollers, ASICs, as well as other signal processors such as A/D converters and the like);

Given the teaching of Stanley, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the circuit and system of Vranish by employing well known or conventional features such as calculation means for providing proximity information, as disclosed by Stanley, in order to determine proximity of an object to be sensed by the sensing electrodes.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vranish in view of van Seeters (US Patent 5,283,528, February 1, 1994, hereinafter referred to as Seeters).

As to claim 14, Vranish discloses an apparatus and methods as discussed in paragraph 6 above. However, Vranish fails to disclose:

The first signal is an integrated square wave.

Seeters discloses:

The first signal is an integrated square wave (Column 4, lines 43 - 48; note that Seeters explicitly discloses the use of an integrated square wave in a capacitive sensor apparatus; note also that the use of square wave signal sources to drive capacitive sensors is well known in capacitive sensor design arts and would have been obvious to persons of ordinary skill in those arts at the time of the invention).

Given the teaching of Seeters, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the circuit and system of Vranish by employing well known or conventional features such as an integrated square wave to drive sensor and guard electrodes, as disclosed by Seeters, in order to more efficiently drive sensor and guard electrodes.

12. Claims 15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vranish in view of Marek (WO8908352, Publication Date 1989-09-08, hereinafter referred to as Marek).

As to claims 15 and 30, Vranish discloses an apparatus and methods as discussed in paragraph 6 above. However, Vranish fails to disclose:

A casing attachable to the body and for enclosing the sensor plates and the first and second guard plates [claim 15];

A vehicle comprising a capacitive sensor [claim 30].

Marek discloses:

A casing attachable to the body and for enclosing the sensor plates and the first and second guard plates [claim 15] (Figure 5a, items 1, 2, 3; note attachment to the car body; note also Figure 5b and Figure 5d, also Figure 5e, clearly suggesting encasement of the sensor plates and guard plates; note also Figures 2 and 3, Items 1, 2, 3, clearly showing sensor and first and second guard plates);

A vehicle comprising a capacitive sensor [claim 30] (Figure 5a, items 1, 2, 3; note mounting to car).

Given the teaching of Marek, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the circuit and system of Vranish by employing well known or conventional features such as a case attachable to the body for enclosing the sensor and guard plates, and a vehicle comprising a

capacitive sensor, as disclosed by Marek, in order to mount and use a capacitive proximity sensor on a vehicle.

Allowable Subject Matter

13. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest, singly or in combination, a capacitive sensor including:

The casing further comprises a recess at an upper end and a recess at a lower end, such that, when the sensor is mounted on the body, the recesses are configured to direct liquid flow flowing down the body to flow generally between the second guard plate and the body upon which the sensor is mounted.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin M. Baldridge whose telephone number is 571 270 1476. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571 272 2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2831

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Diego Gutierrez/ Supervisory Patent Examiner, Art Unit 2831

/Benjamin M Baldridge/ Examiner, Art Unit 2831